

CDM4-650

**SURFACE MOUNT SILICON
N-CHANNEL
MEDIUM POWER MOSFET
4.0 AMP, 650 VOLT**



DPAK CASE



www.centrasemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CDM4-650 is a 650 volt N-Channel MOSFET designed for high voltage, fast switching applications such as Power Factor Correction (PFC), lighting and power inverters. This MOSFET combines high voltage capability with low $r_{DS(ON)}$, low threshold voltage, and low gate charge for optimal efficiency.

MARKING: FULL PART NUMBER

APPLICATIONS:

- Power Factor Correction
- Alternative energy inverters
- Solid state lighting

FEATURES:

- High voltage capability ($V_{DS}=650V$)
- Low gate charge ($Q_{GS}=3.0nC$)
- Low $r_{DS(ON)}$ (2.44Ω)

MAXIMUM RATINGS: ($T_A=25^\circ C$ unless otherwise noted)

	SYMBOL		UNITS
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	30	V
Continuous Drain Current (Steady State)	I_D	4.0	A
Maximum Pulsed Drain Current, $t_p=10\mu s$	I_{DM}	16	A
Continuous Source Current (Body Diode)	I_S	4.0	A
Maximum Pulsed Source Current (Body Diode)	I_{SM}	16	A
Single Pulse Avalanche Energy (Note 1)	E_{AS}	202	mJ
Power Dissipation	P_D	0.62	W
Power Dissipation ($T_C=25^\circ C$)	P_D	77	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-55 to +150	$^\circ C$
Thermal Resistance	θ_{JC}	1.62	$^\circ C/W$
Thermal Resistance	θ_{JA}	110	$^\circ C/W$

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ C$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=30V, V_{DS}=0$		10	100	nA
I_{DSS}	$V_{DS}=650V, V_{GS}=0$		0.03	1.0	μA
BV_{DSS}	$V_{GS}=0, I_D=250\mu A$	650			V
$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	3.4	4.0	V
V_{SD}	$V_{GS}=0, I_S=4.0A$		0.87	1.4	V
$r_{DS(ON)}$	$V_{GS}=10V, I_D=2.0A$		2.44	2.7	Ω
C_{rss}	$V_{DS}=25V, V_{GS}=0, f=1.0MHz$		1.0		pF
C_{iss}	$V_{DS}=25V, V_{GS}=0, f=1.0MHz$		463		pF
C_{oss}	$V_{DS}=25V, V_{GS}=0, f=1.0MHz$		60		pF

Notes: (1) $L=30mH, I_{AS}=3.6A, V_{DD}=50V, R_G=25\Omega, \text{Initial } T_J=25^\circ C$

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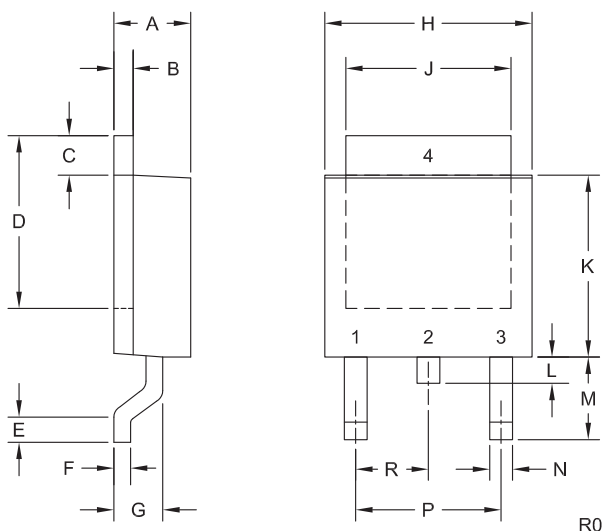


ELECTRICAL CHARACTERISTICS - Continued: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	TYP	UNITS
$Q_{g(\text{tot})}$	$V_{DS}=520\text{V}$, $V_{GS}=10\text{V}$, $I_D=4.0\text{A}$ (Note 2)	11.4	nC
Q_{gs}	$V_{DS}=520\text{V}$, $V_{GS}=10\text{V}$, $I_D=4.0\text{A}$ (Note 2)	3.0	nC
Q_{gd}	$V_{DS}=520\text{V}$, $V_{GS}=10\text{V}$, $I_D=4.0\text{A}$ (Note 2)	4.7	nC
t_d	$V_{DD}=325\text{V}$, $I_D=4.0\text{A}$, $R_G=25\Omega$ (Note 2)	9.0	ns
t_r	$V_{DD}=325\text{V}$, $I_D=4.0\text{A}$, $R_G=25\Omega$ (Note 2)	23	ns
t_s	$V_{DD}=325\text{V}$, $I_D=4.0\text{A}$, $R_G=25\Omega$ (Note 2)	23	ns
t_f	$V_{DD}=325\text{V}$, $I_D=4.0\text{A}$, $R_G=25\Omega$ (Note 2)	21	ns
t_{rr}	$V_{GS}=0$, $I_S=4.0\text{A}$, $di/dt=100\text{A}/\mu\text{s}$ (Note 2)	266	ns
Q_{rr}	$V_{GS}=0$, $I_S=4.0\text{A}$, $di/dt=100\text{A}/\mu\text{s}$ (Note 2)	2.24	μC

Notes: (2) Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

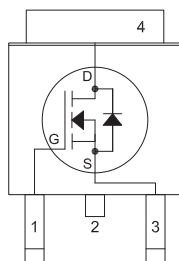
DPAK CASE - MECHANICAL OUTLINE



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.083	0.108	2.10	2.75
B	0.016	0.032	0.40	0.81
C	0.035	0.063	0.89	1.60
D	0.203	0.228	5.15	5.79
E	0.020	-	0.51	-
F	0.018	0.024	0.45	0.60
G	0.051	0.071	1.30	1.80
H	0.248	0.268	6.30	6.81
J	0.197	0.217	5.00	5.50
K	0.209	0.245	5.30	6.22
L	0.025	0.040	0.64	1.02
M	0.090	0.115	2.30	2.91
N	0.012	0.045	0.30	1.14
P	0.180		4.60	
R	0.090		2.30	

DPAK (REV: R0)

PIN CONFIGURATION



LEAD CODE:

- 1) Gate
 - 2) Drain
 - 3) Source
 - 4) Drain
- Pin 2 is common to the tab (4)

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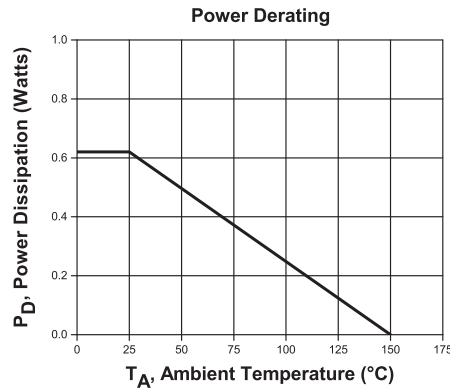
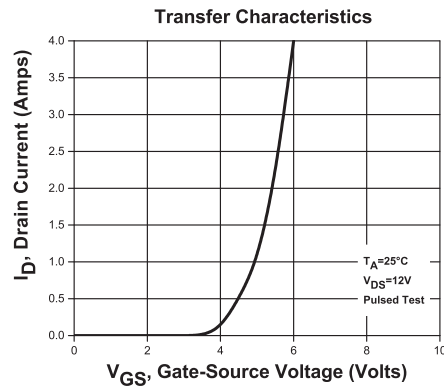
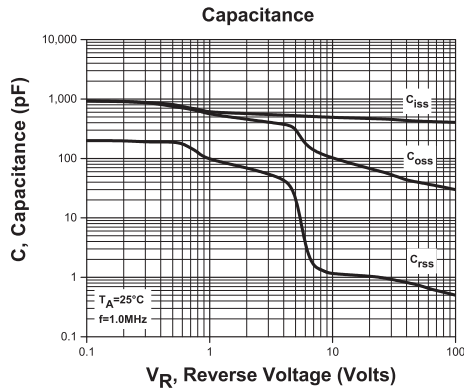
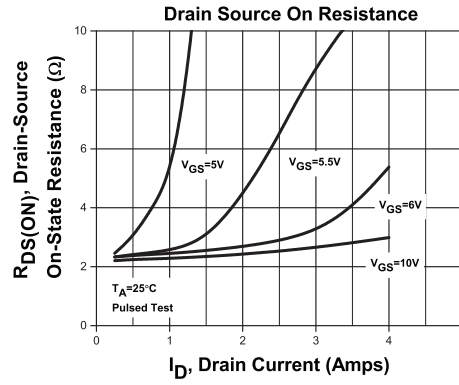
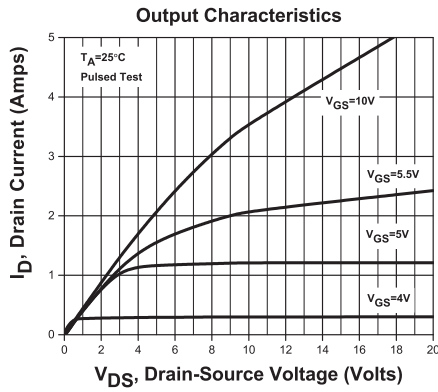
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TYPICAL ELECTRICAL CHARACTERISTICS



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- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

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- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
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- Application notes
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