Exploring the performance characteristic differences between MOSFET-based CLDs and traditional JFET CLDs

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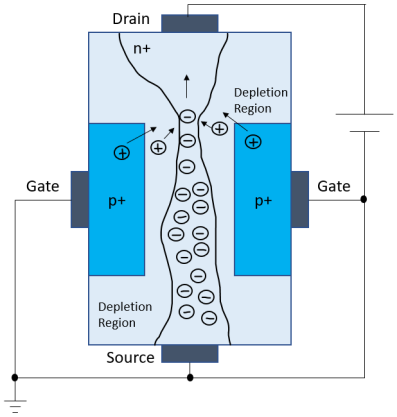
Purpose of the Study

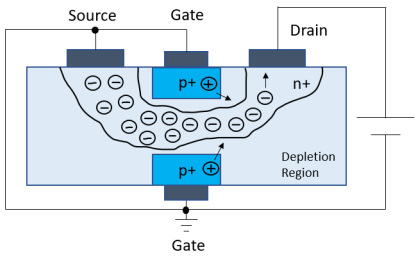
Current limiting diodes (CLDs), also called constant current diodes and current regulating diodes, have traditionally been constructed using N-Channel junction field effect transistor (N-Ch JFET) topologies. The main difference in construction between a standard N-Ch JFET and a CLD is the institution of a short between the gate and source. This effectively makes the JFET a two-leaded device rather than a three-leaded device, leaving a drain terminal and a combined gate-source terminal. Applying a positive potential to the drain relative to the gate-source forms a depletion region in the n-channel of the JFET. As the potential is increased, the depletion region expands, ultimately pinching off the electrons flowing towards the positively charged drain terminal **(Figure 1)**. This marks the ohmic to saturated transition point in the I-V relationship of the FET. While this is normally viewed as the main real-world limitation of FETs, it is the working principle of the CLD. Once in saturation, any voltage applied within the device's power limitations will equate to the same, regulated current output; i.e. the "limiting" current. This is an extremely useful property, as it allows for active current regulation for any applied rail voltage value. Simultaneously, CLDs present a high input impedance, which equates to higher levels of efficiency for amplification circuits.

Figure 1:
Traditional JFET CLD Structure



No device comes without its caveats, and the traditional N-Ch JFET structured CLD is no different. As the device heats up during operation, either with a high applied voltage or due to the ambient environment, regulated current performance will degrade. The increase in temperature causes the generation of free holes in the P-type regions surrounding the gate terminals. These free holes then travel to recombine with the electrons flowing through the N-channel, thus resulting in a lower limiting current. There are other JFET CLD structures available however none are completely infallible. One implementation is the use of the lateral N-Ch JFET. By shrinking the N-channel height, pinch-off occurs at a lower positive potential difference between drain and gate-source. This yields a larger acceptable applied voltage range before the device heats too rapidly and current degradation occurs **(Figure 2)**. Another common implementation is the use of a parallel resistor to compensate for heat generation and to prevent current degradation. Both cases are temporary adjustments rather than solutions, however. The lateral N-Ch JFET may give the user a larger applied voltage range, but the ambient environment may be at elevated temperatures, or it may be a high voltage application. The parallel compensation resistor will relieve the device at a particular applied voltage, but if that voltage were to increase or decrease, so too would the required value of the compensation resistor. Given the flaws in these solutions, it became clear that a true solution to this problem would require a re-design from the ground-up.

Figure 2:
Lateral JFET CLD Structure



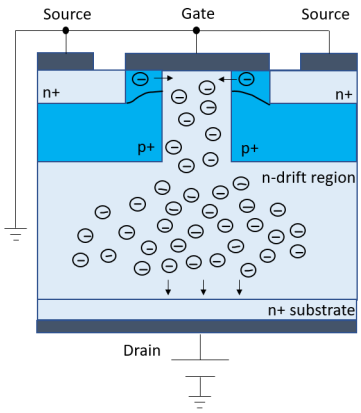
Technical Design

This solution materialized as a new device type that borrows from a N-Ch MOSFET structure. This new type of design features all of the traits necessary to ensure essentially no current degradation due to temperature increase, whether ambient or from a large applied voltage. In this literary work, the technical details of the MOSFET-based CLD are presented and discussed. To validate the effectiveness of this design, two versions of the MOSFET-based CLD and two versions of the JFET CLD are evaluated in the same application circuit, with a detailed data comparison highlighting the difference in performance between the two device types.

To ensure that the N-Ch MOSFET CLD structure operates without current degradation due to temperature increase, inducing optimal charge carrier movement becomes the most important design factor. This follows the same thought process as the lateral N-Ch JFET design. The structure design starts with a similar approach; the technology is converted into a two-lead device by constructing a short between the gate and source. This combined gate-source terminal then acts as the cathode of the device. In the N-Ch JFET CLD, since both the source and drain are constructed on the same side, electrons travel from source to drain in lateral fashion as the potential applied to the drain terminal relative to the gate-source terminal is increased. In the N-Ch MOSFET structure, the gate terminal and gate passivation is sandwiched between two source terminals. The gate passivation contacts the device body and p-type regions that surround the source terminals. The drain terminal is then placed on the opposite side of the device.

When a positive potential is applied to the drain terminal in the N-Ch MOSFET, an N-channel forms in the P-type region between the sources and gate passivation. This allows for electrons to flow from the sources, through the P-type region, to the body of the device **(Figure 3)**. Within a few volts of positive potential applied to the drain, the depletion region will have expanded enough to regulate current flow. As with lateral JFET design, this is due to the height of the channel being decreased, thus lowering the pinch-off voltage of the device. The low pinch-off means an expanded input voltage window for regulated current, allowing for design engineers to achieve the full output current even in low voltage systems. This leads to less power dissipation required in steady state operation and overall less stress on the CLD. However, as with JFETs, if the charge carrier movement was solely lateral, devices would have an expanded input voltage window but still be subject to free-hole movement at high voltages due to thermal inefficiency. This is because the P-type region that this channel forms in is very small and incapable of dissipating heat at a fast rate.

Figure 3:
N-Ch MOSFET-based CLD Structure



After passing through the P-type region, the electrons are attracted to the overwhelmingly positive potential of the drain and flow towards it. This is why the drain terminal must be placed on the opposite side of the body and not on the same side as the gate-source. By placing the drain terminal directly opposite the gate-source, vertical charge carrier movement is induced for the electrons that have just moved to drift region of the device. This large drift region is able to easily withstand the thermal stress generated due to the electrons flowing across it. Since heat can now be dissipated without issue, there are no free holes generated from excessive temperatures. Thus, no recombination occurs in the vertical channel of the body.

While channel height is a squared, numerator term in the expression for pinch-off voltage, implant doping concentration is also a numerator term. This means that doping concentration can be adjusted as a secondary procedure for tweaking the pinch-off voltage of CLDs. Since adjusting the doping also has a large impact on parasitics, it is typical that it be adjusted for refinement purposes only. If adjusted as the primary means for achieving the desired pinch-off characteristics, it could impact the integrity of other parametric properties.

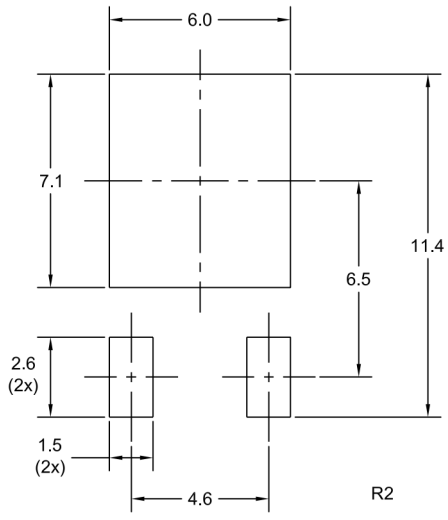
Circuit and Experiment

In order to validate the performance characteristics of the MOSFET-based CLD compared to the JFET CLD, a demonstration was designed. **Table 1** is a side-by-side comparison illustrating the specifics of the packages and printable circuit boards (PCBs) used in the demonstration. Both boards were configured with extra vias to allow for an ammeter to be placed in series with the CLDs. The device pad layouts follow the recommended Central Semiconductor D-PAK board footprint **(Figure 4)**.

Table 1:
PCB Layout Information

Parameter	MOSFET-based CLD	JFET CLD
Board Laminate	FR-4	FR-4
Board Length	2.5 inches	2.5 inches
Board Width	3.8 inches	3.8 inches
Board Thickness	4 layers	4 layers
Layer Material	1oz. Copper	1oz. Copper
Trace Width	20 mils	20 mils
Pad Plating	Tin/Lead	Tin/Lead
Pad Style	Thermal	Thermal
Pad Width	56 mils	56 mils
Via Width	29 mils	29 mils
Footprints	D-PAK	D-PAK

Figure 4:
Central recommended D-PAK layout (in mm)



The first board design in **Figure 5** is for the MOSFET-based CLDs in **Table 2**, which have a back-tab anode and first pin cathode. The top row of footprints are for Central's CDCLD500 and the bottom row of footprints are for Central's CDCLD120.

Figure 5:
CEN (MOSFET) PCB Design

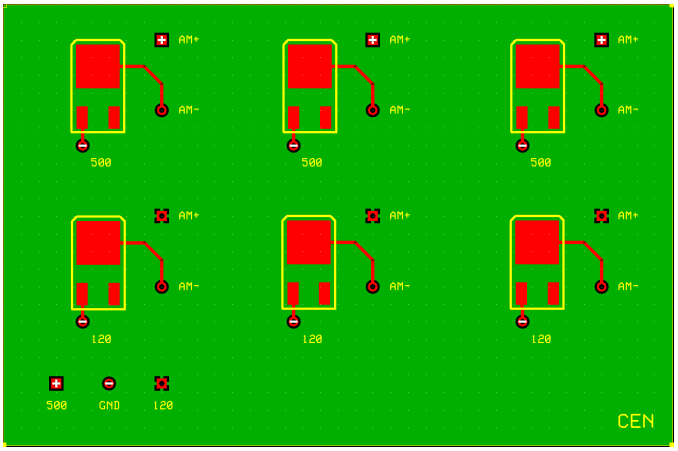


Table 2:
Parametric Limits of CEN board CLDs

Parameter	CDCLD120	CDCLD500
Regulated Current	Typ 120mA	Typ 500mA
Max Voltage (Si Limit)	50V	50V
Board Width	3.8 inches	3.8 inches

The second board design in **Figure 6** is for the JFET CLDs in **Table 3**, which has a back-tab cathode and first pin anode. The top row of footprints are for the 350 JFET CLD and the bottom row of footprints are for the 160 JFET CLD.

The first portion of the demonstration tests the standard IV curve of each device. The purpose is to exemplify the early pinch-off voltage of the MOSFET-based CLD. To present a fair comparison, low current devices, i.e. 120mA MOSFET and 100mA JFET, were paired together. Similarly, the higher current devices, i.e. 500mA MOSFET and 350mA JFET, were paired together. Three devices per current value were used to take the data, with the results averaged into one current per voltage measurement. Additionally, each measurement was taken after 30 seconds of settling time at each applied voltage value.

Figure 6:
Competitor (JFET) PCB Design

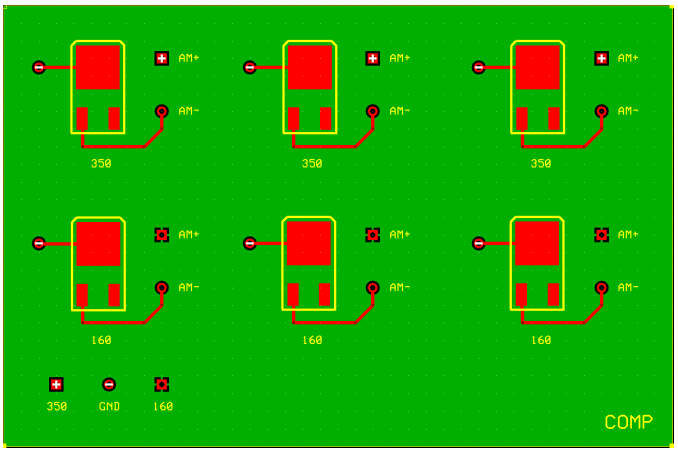


Table 3:
Parametric Limits of Competitor board CLDs

Parameter	JFET CLD 160	JFET CLD 350
Regulated Current	Typ 100mA	Typ 350mA
Max Voltage (Si Limit)	45V	50V
Board Width	3.8 inches	3.8 inches

In **Figure 7**, the CDCLD120 has a limiting voltage of 1.3V and reaches its nominal current at 5.2V applied. By comparison, the 100mA JFET has a limiting voltage of 2.1V and reaches its nominal current at 13.2V applied. As previously noted, this earlier pinch-off voltage is the desired effect from implementing a lateral channel structure. The same result can be seen for the high current models in **Figure 8**. The CDCLD500 has a limiting voltage of 0.9V and reaches its nominal current at 2V applied. The 350mA JFET has a limiting voltage of 1.9V and reaches its nominal current at 5V applied. Using this data, it can be determined that the MOSFET-based CLD limiting voltage occurs at an applied voltage that is only 54% of the required JFET limiting voltage. Similarly, the pinch-off of the MOSFET-based CLD occurs at an applied voltage that is only 40% of the required JFET pinch-off voltage.

The most obvious real-world benefit of an early pinch-off voltage is enhanced application versatility. The lower the pinch-off voltage, the wider the applied voltage window for meeting the nominal current. This makes the device applicative to more designs by allowing engineers flexibility in the supply voltage used to power MOSFET-based CLDs. The secondary benefit, which was the original purpose of integrating the lateral channel into CLDs, is the indirect limiting of current degradation in the device. The less voltage required to operate the CLD at its nominal regulated current, the less power being dissipated by the device. With less power being dissipated, there is less self-induced rapid heat generation.

The second portion of the demonstration tests the settling time of each device, which is typically 30 to 60 seconds. The purpose of this demonstration is to show the small change in the regulated current from test start to test finish in MOSFET-based CLDs. An applied voltage was selected that would ensure each CLD was dissipating the same amount of power as its counterpart. For the low current devices, nominal currents were close enough to apply 25V to both devices, yielding about 2.9W of power dissipation per device at test start. For the high current devices, 10V was selected for Central's CDCLD500 and 11.4V was selected for the 350mA JFET, yielding about 5.2W of power dissipation per device at test start.

Figure 7:
Low Current IV Curve

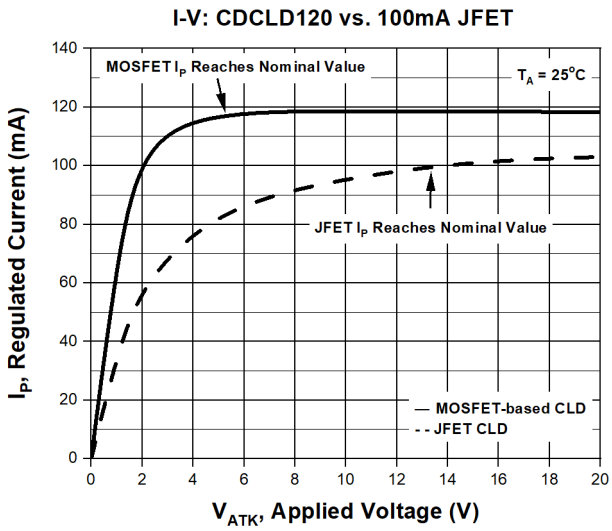
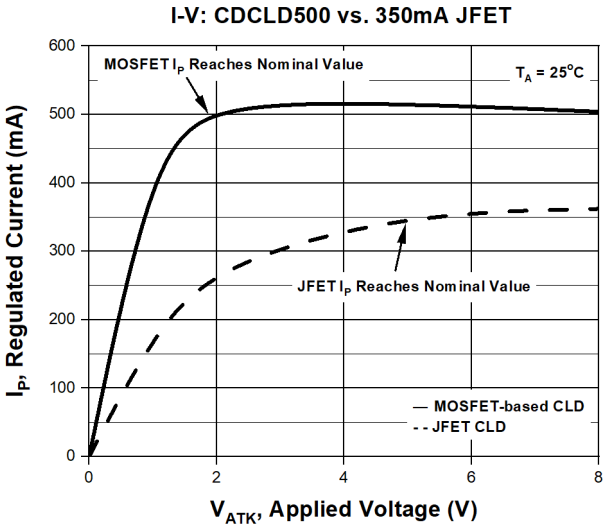


Figure 8:
High Current IV Curve



In **Figure 9**, Central's CDCLD120 experiences a delta shift of -1.1mA. Comparatively, the 100mA JFET experiences a delta shift of -7.2mA. Similarly, in **Figure 10**, the CDCLD500 undergoes a delta shift of -40mA and the 350mA JFET undergoes a delta shift of -104mA. As noted previously, these shifts are due to the thermal stresses introduced to the device during operation. As the device heats, free holes are generated, and recombine with electrons in the channel. However, as theorized earlier, the MOSFET-based CLD has a much-improved delta shift compared to the traditional JFET technology. The data confirms this, as the low current JFET CLD degrades 6.5 times as much as the MOSFET-based CLD, and the high current JFET CLD degrades 2.5 times as much as the MOSFET-based CLD. The large drift region of the MOSFET, which induces vertical charge flow over a large area, directly translates to improved heat dissipation. The improved heat dissipation then directly explains the much-improved delta-shift in regulated current. Thus, the overall design theory of the MOSFET-based CLD is proven effective.

In real-world applications, this is a major benefit. One of the most unpredictable measures engineers have to take with their designs is derating based on operating conditions and temperature. Knowing that CLDs won't degrade heavily over time helps ensure that the system functions as intended, without having to introduce multiple precautions.

The final portion of the demonstration tests the effects of ambient temperature on the regulated output current of each device. The purpose of this demonstration is to show that ambient temperature has a much more significant effect on JFET CLDs than it does on MOSFET-based CLDs. The applied voltages used were the same as the settling time test, done to ensure that each CLD was dissipating the same amount of power as its counterpart.

Figure 9:
Low Current Settling Time

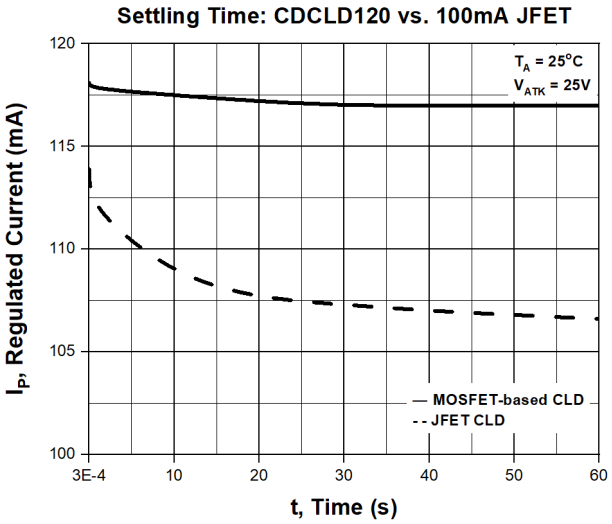
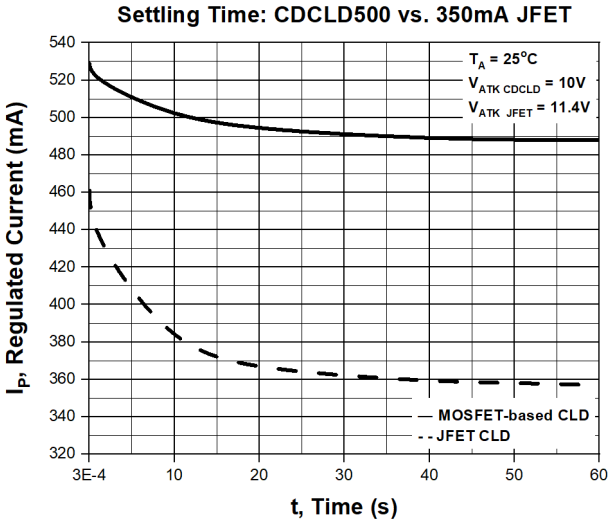


Figure 10:
High Current Settling Time



In **Figure 11**, Central's CDCLD120 experiences a delta shift of -6.4mA, a 58% reduction in current degradation from the -15.1mA delta shift of the 100mA JFET. Similarly, in **Figure 12**, the CDCLD500 undergoes a delta shift of -32.9mA, a 66% reduction in current degradation from the -97.8mA delta shift of the 350mA JFET. As previously noted, these shifts are due to the thermal stresses introduced to the device during operation. Similar to self-induced heating during operation, an increase in ambient temperature generates free holes that recombine with electrons in the channel. As previously stated, the large drift region of the MOSFET helps dissipate heat immediately, thus generating less free holes and preventing significant current degradation.

Figure 11:
Low Current Temperature Induced Degradation

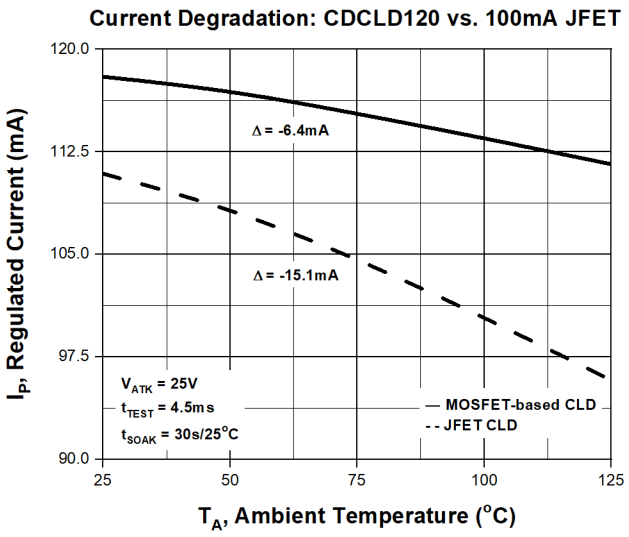
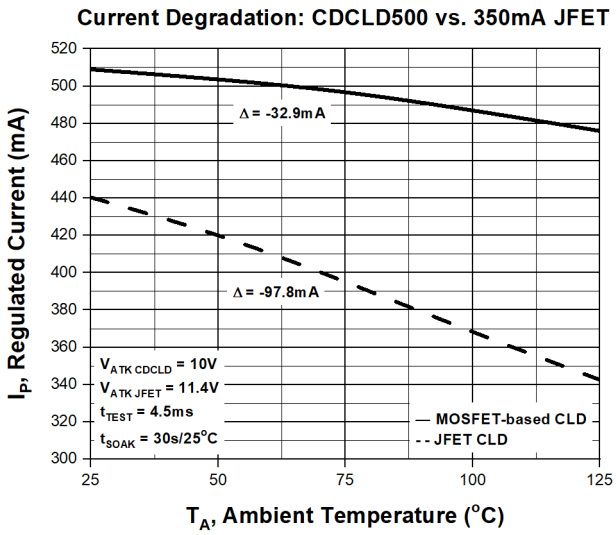


Figure 12:
High Current Temperature Induced Degradation



Conclusion

Very rarely are "perfect" operating conditions present in an application. As the number of dynamic variables increases, more necessary precautions become required. This is the only way to effectively ensure proper operation on a component and system level. One of the most common and uncontrollable operating conditions that varies is ambient temperature. The small amount of change that MOSFET-based CLDs demonstrate over a large ambient temperature range provides a sense of stability previously unachievable with conventional CLD technology, and ultimately leads to less necessary compensation. Not all applications will require the enhanced stability levels afforded by the MOS based topology; for less sensitive applications, conventional JFET-based technology is likely sufficient. For more sensitive applications, however, the MOS based approach is as close to an ideal solution as can be achieved with a single component.

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