

Product / Process Change Notice

Parts Affected:

Chip process CP209, N-Channel JFETS, wafers and bare die.

Extent of Change:

The CP209 wafer process has been discontinued and is being replaced with the CP264V wafer process. See Figures 1 and 2 for details.

Reason for Change:

The CP209 wafer process has been replaced in order to enhance manufacturing process controls and device performance. This change will help to ensure an undisrupted supply of product.

Effect of Change:

The CP264V wafer process meets all electrical specifications of the individual devices listed on the following page.

Qualification:

Test	Condition	Failure rate
High Temperature Storage Life/ bake test.	150°C (-0/+10)°C, 1000 hours. JESD22-A103	0/77
Temperature Cycling	T= -65°C to +150°C 1000 cycles. Dwell time = 15 min. JESD22-A104 & MIL-STD-750 TM1051	0/77
High Temperature Gate Bias (HTGB)	T=125°C, t=1000 hours, Bias at V _{GS} from gate to source with source and drain shorted JESD22-A108	0/77
Highly Accelerated Temperature and Humidity Stress Test (HAST)	T = 110°C, RH = 85%, and t = 264 hours. Bias conditions per device specification sheet. JESD22-A110	0/77

Earliest Effective Date of Change:

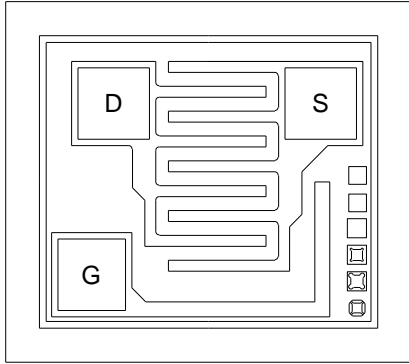
August 20, 2021

Inventory Availability

Existing inventory will be shipped until depleted.

PCN #221
Notification Date:
June 17, 2021

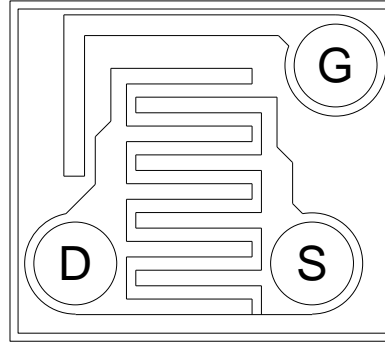
Figure 1: CP209 Chip Geometry (Discontinued)



BACKSIDE GATE

Wafer Diameter: 5 inch
Die Size: 18 x 16 mils
Die Thickness: 7.9 mils
Bond Pad Size (Drain): 3.0 x 3.0 mils
Bond Pad Size (Source): 3.0 x 3.0 mils
Bond Pad Size (Gate): 3.0 x 3.0 mils
Topside Metal: Al-Si (17,000Å)
Backside Metal: Au (12,000Å)

Figure 2: CP264V Chip Geometry



BACKSIDE GATE R0

Wafer Diameter: 5 inch
Die Size: 17.1 x 15.1 mils
Die Thickness: 7.9 mils
Bond Pad Size (Drain): 3.7 mils Diameter
Bond Pad Size (Source): 3.7 mils Diameter
Bond Pad Size (Gate): 3.7 mils Diameter
Topside Metal: Al-Si (17,000Å)
Backside Metal: Au (12,000Å)

Part Numbers Affected:

2N4222	2N5457	2N5458	2N5459
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As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor's Product/Process Change Notification (PCN).

Company Name:	
Address:	
Printed Name:	
Title:	
Signature:	
Date:	