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**PCN # 202_Rev 1**

**Revision 1 Notification Date: June 4, 2021**

**Original Notification Date: January 28, 2021**

# Product / Process Change Notice

**Revision 1 June 4, 2021:** Issued to update the Effective Date of Change and add Inventory Availability.

## Parts Affected:

Chip process CP216, N-Channel field effect transistors, wafers and bare die.

## Extent of Change:

The CP216 wafer process has been discontinued and is being replaced with the CP226V wafer process. See Figures 1 and 2 for details.

## Reason for Change:

The CP216 wafer process has been replaced in order to enhance manufacturing process controls and device performance. This change will help ensure an undisrupted supply of product.

## Effect of Change:

The CP226V wafer process meets all electrical specifications of the individual devices listed on the following page.

## Qualification:

| Test | Condition | Failure rate |
|---|---|---|
| **High Temperature Storage Life/ bake test.** | 150°C (-0/+10)°C, 1000 hours.<br>**JESD22-A103** | 0/77 |
| **Temperature Cycling** | T= -65°C to +150°C<br>1000 cycles. Dwell time = 15 min.<br>**JESD22-A104 & MIL-STD-750 TM1051** | 0/77 |
| **High Temperature Gate Bias (HTGB)** | T=125°C, t=1000 hours, Bias at V_GS from gate to source with source and drain shorted<br>**JESD22-A108** | 0/77 |
| **Highly Accelerated Temperature and Humidity Stress Test (HAST)** | T = 110°C, RH = 85%, and t = 264 hours.<br>Bias conditions per device specification sheet.<br>**JESD22-A110** | 0/77 |
| **Intermittent Operational Life (IOL)** | Ta=25°C, ΔTj>=100°C<br>Bias conditions per device datasheet<br>Number of Cycles:<br>for ΔTj>=100°C: 60000/(x+y)<br>for ΔTj>=125°C: 30000/(x+y)<br>x = time on ; y = time off (x , y >= 2 minutes)<br>**MIL-STD-750 TM1037 & JESD22-A105** | 0/77 |

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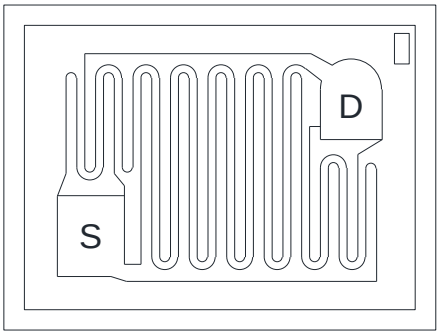
## Earliest Effective Date of Change:

April 28, 2021

## Inventory Availability

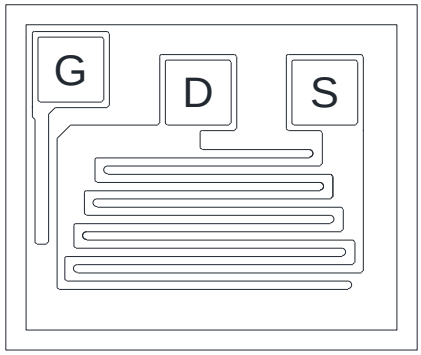
Existing inventory will be shipped until depleted.

**Figure 1: CP216 Chip Geometry (Discontinued)**




| | |
|---|---|
| Wafer Diameter: | 4 inch |
| Die Size: | 21 x 16 mils |
| Die Thickness: | 7.9 mils |
| Bond Pad Size (Drain): | 3.3 x 4.5 mils |
| Bond Pad Size (Source): | 3.3 x 4.5 mils |
| Topside Metal: | Al (10,000Å) |
| Backside Metal: | Au (3,250Å) |

**Figure 2: CP226V Chip Geometry**




| | |
|---|---|
| Wafer Diameter: | 5 inch |
| Die Size: | 20 x 17 mils |
| Die Thickness: | 7.1 mils |
| Bond Pad Size (Drain): | 3.2 x 3.2 mils |
| Bond Pad Size (Source): | 3.2 x 3.2 mils |
| Bond Pad Size (Gate): | 3.2 x 3.2 mils |
| Topside Metal: | Al (30,000Å) |
| Backside Metal: | Au (9,000Å) |

**Part Numbers Affected:**

| | | | |
|---|---|---|---|
| CEN1280 | 2N3972 | 2N4858 | CP216-2N4392-CM |
| CMPF4391 | 2N4091 | 2N4858A | CP216-2N4392-CT |
| CMPF4392 | 2N4092 | 2N4859 | CP216-2N4392-WN |
| CMPF4393 | 2N4093 | 2N4859A | CP216-2N4393-CM |
| PN4091 | 2N4391 | 2N4860 | CP216-2N4393-CT |
| PN4092 | 2N4392 | 2N4860A | CP216-2N4393-WN |
| PN4093 | 2N4393 | 2N4861 | CP216-2N4856-CM |
| PN4391 | 2N4856 | 2N4861A | CP216-2N4856-CT |
| PN4392 | 2N4856A | | CP216-2N4856-WN |
| PN4393 | 2N4857 | | |
| 2N3971 | 2N4857A | | |

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As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor's Product/Process Change Notification (PCN).

| | |
|---|---|
| Company Name: | |
| Address: | |
| | |
| | |
| Printed Name: | |
| Title: | |
| Signature: | |
| Date: | |