

**PCN #175**  
**Notification Date:**  
**August 14, 2019**

**Product / Process Change Notice**

**Parts Affected:**

Chip process CP147, NPN Darlington transistors, wafers and bare die

**Extent of Change:**

The CP147 wafer process has been discontinued and replaced with the CP247 wafer process. See figures 1 and 2 for details.

**Reason for Change:**

The CP147 wafer process has been replaced by the CP247 wafer process in order to enhance the manufacturing process controls and performance. In addition, this change is being made to ensure undisrupted supply of product, moving forward.

**Effect of Change:**

The wafer process meets all electrical specifications of the individual devices listed on the following page.

**Qualification:**

P/N: CP247 Chip Process

Package: TO-3

| No.      | Test                                 | Conditions<br>(Reference standards are in bold)   | Qty | Pass/Fail | Test Results |
|----------|--------------------------------------|---|-----|-----------|--------------|
| <b>1</b> | <b>Device Life Tests</b>             |   |     |           |              |
| a        | High Temperature Reverse Bias (HTRB) | T=125°C, t = 1000 hours<br>Bias conditions per device datasheet<br><b>JESD22-A108</b>                 | 77  | Pass      | 77/77        |
| b        | High Temperature Storage Life (HTSL) | T=150°C, t = 1000 hours<br><b>JESD22-A103</b>   | 77  | Pass      | 77/77        |
| C        | Thermal Shock                        | 100 cycles, dwell time = 5 min,<br>-65°C to +150°C, max transfer time = 20 sec.<br><b>JESD22-A106</b> | 77  | Pass      | 77/77        |
| D        | Temperature Cycling (TC)             | -55°C -+175°C, Tdwell = 15min,<br>1000 cycles   | 77  | Pass      | 77/77        |

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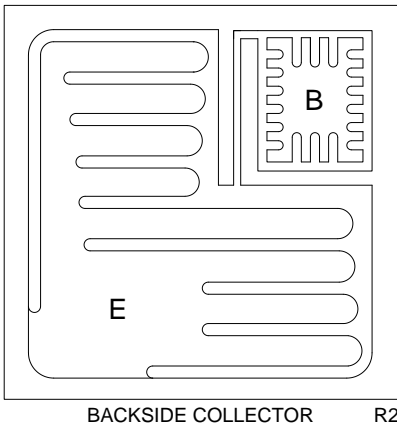
**Effective Date of Change:**

Existing Inventory of chip process CP147 will be shipped until depleted.

**Sample Availability:**

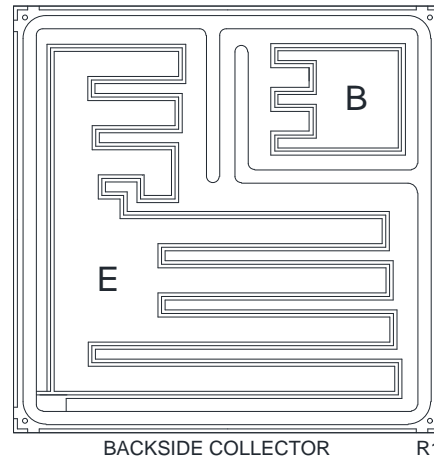
Please contact your salesperson or manufacturer's representative for samples.

**Figure 1: CP147 Chip Geometry (Discontinued)**



Wafer Diameter: 5 inch  
Die Size: 195 x 195 mils  
Die Thickness: 11.4 mils  
Bond Pad Size (Base): 28 x 28 mils  
Bond Pad Size (Emitter): 70 x 44 mils  
Topside Metal: Al (60,000Å)  
Backside Metal: Ti/Ni/Au (1,000Å/4,000Å/500Å)

**Figure 2: CP247 Chip Geometry**



Wafer Diameter: 5 inch  
Die Size: 211 x 211 mils  
Die Thickness: 12.5 mils  
Bond Pad Size (Base): 49 x 41 mils  
Bond Pad Size (Emitter): 60 x 50 mils  
Topside Metal: Al (50,000Å)  
Backside Metal: Ti/Ni/Ag(1,000Å/6,000Å/10,000Å)

**Part Numbers Affected:**

|                  |                  |
|------------------|------------------|
| CP147-MJ11016-CT | CP147-CEN1104-CT |
| CP147-MJ11016-WN | CP147-2N6284-CT  |
| CP147-2N6284-CM  |                  |



145 Adams Avenue, Hauppauge, NY 11788 USA  
Tel: (631) 435-1110 • Fax: (631) 435-1824  
[www.centralsemi.com](http://www.centralsemi.com)  
<mailto:processchange@centralsemi.com>  
<http://www.centralsemi.com/processchange>

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As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor's Product/Process Change Notification (PCN).

|               |  |
|---------------|--|
| Company Name: |  |
| Address:      |  |
|               |  |
|               |  |
| Printed Name: |  |
| Title:        |  |
| Signature:    |  |
| Date:         |  |