**Product / Process Change Notice**

**Parts Affected:**

Chip process CP210, N-Channel JFETs, wafers and bare die

**Extent of Change:**

The CP210 wafer process has been discontinued and replaced with the CP232V wafer process. See figures 1 and 2 for details.

**Reason for Change:**

The CP210 wafer process has been replaced by the CP232V wafer process in order to enhance the manufacturing process controls and performance. In addition, this change is being made to ensure undisrupted supply of product, moving forward.

**Revision 1** **September 27, 2019:** Issued to include additional devices not on the initial PCN release. Newly added devices are shown in the “Part Numbers Affected” section on page 3 marked with \*.

**Effect of Change:**

The wafer process meets all electrical specifications of the individual devices listed on the following page.

**Qualification:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | P/N: | CP232V Chip Process |  | Package: | TO-72 |
|  |  |  |  |  |  |  |
| **No.** | **Test** | **Conditions**(Reference standards are in bold) | **Qty** | **Pass/Fail** | **Test Results** |
| **1** | **Device Life Tests** |
|  | a | **High Temperature Gate Bias (HTGB)** | T=125°C, t = 1000 hours100%, VGS=35V, Source and Drain Shorted **JESD22-A108** | 77 | Pass | 77/77 |
|  | b | **High Temperature Storage Life (HTSL)** | T=150°C, t = 1000 hours**JESD22-A103** | 77 | Pass | 77/77 |
|  | C | **Thermal Shock** | 100 cycles, dwell time = 5 min, -65°C to +150°C, max transfer time = 20 sec.**JESD22-A106** | 77 | Pass | 77/77 |
|  | D | **Temperature Cycling (TC)** | -65°C to +150°C, Tdwell = 15min, 1000 cycles | 77 | Pass | 77/77 |

**Effective Date of Change:**

Existing Inventory of chip process CP210 will be shipped until depleted.

**Sample Availability:**

Please contact your salesperson or manufacturer’s representative for samples.

|  |  |
| --- | --- |
| **Figure 1: CP210 Chip Geometry (Discontinued)**  | **Figure 2: CP232V Chip Geometry** |
|  |  |
| Wafer Diameter | 5 inch | Wafer Diameter | 5 inch |
| Die Size | 15 x 15 mils | Die Size | 14 x 14 mils |
| Die Thickness | 8.0 mils | Die Thickness |  7.1 mils |
| Bond Pad Size (Gate): | 4.0 x 3.2 mils | Bond Pad Size (Gate): | 2.95 x 3.46 mils |
| Bond Pad Size (Source): | 4.0 x 3.2 mils | Bond Pad Size (Source): | 3.46 x 3.46 mils |
| Bond Pad Size (Drain): | 4.0 x 3.2 mils | Bond Pad Size (Drain): | 3.15 x 3.46 mils |
| Topside Metal: | Al (30,000Å) | Topside Metal: | Al-Si (17000Å) |
| Backside Metal: | Au (6,000Å) | Backside Metal: | Au-As (9000Å) |
| **Part Numbers Affected:** \* Revision 1 September 27, 2019 newly added devices |
| 2N4416A | CP210-2N4416-CM | 2N3819\* |  |
| 2N4416 | CP210-2N4416-CT | 2N5486\* |  |
| CMPF4416A | CP210-2N4416A-CM | 2N5952\* |  |
| CEN835  | CP210-2N4416A-CT |  |  |
| CMPF5485 | CP210-2N4416A-WN |  |  |
| CMPF5486 | CP210-CEN1308-CT |  |  |
| CEN1165 | CP210-2N5486-CT |  |  |

As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor’s Product/Process Change Notification (PCN).

|  |  |
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| Company Name: |  |
| Address: |  |
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|  |
| Printed Name: |  |
| Title: |  |
| Signature: |  |
| Date: |  |