

**Product / Process Change Notice**

**Parts Affected:**

Chip process CP688, P-Channel JFETs, wafers and bare die

**Extent of Change:**

The CP688 wafer process has been discontinued and replaced with the CP613V wafer process. See figures 1 and 2 for details.

**Reason for Change:**

The CP688 wafer process has been replaced by the CP613V wafer process in order to enhance the manufacturing process controls and performance. The wafer size has increased from 4 inch to 5 inch to improve throughput. In addition, this change is being made to ensure uninterrupted supply of product, moving forward.

**Effect of Change:**

The wafer process meets all electrical specifications of the individual devices listed on the following page.

**Qualification:**

P/N: CP613V Chip Process Package: SOT-23

No.	Test	Conditions (Reference standards are in bold)	Qty	Pass/Fail	Test Results
<b>1</b>	<b>Device Life Tests</b>				
a	High Temperature Gate Bias (HTGB)	T=125°C, t = 1000 hours 100%, VGS=30V, Source and Drain Shorted <b>JESD22-A108</b>	77	Pass	77/77
b	High Temperature Storage Life (HTSL)	T=150°C, t = 1000 hours <b>JESD22-A103</b>	77	Pass	77/77
C	Thermal Shock	100 cycles, dwell time = 5 min, -65°C to +150°C, max transfer time = 20 sec. <b>JESD22-A106</b>	77	Pass	77/77
D	Temperature Cycling (TC)	-65°C -+150°C, Tdwell = 15min, 1000 cycles	77	Pass	77/77

**PCN #172**  
**Notification Date:**  
**21 May 2019**

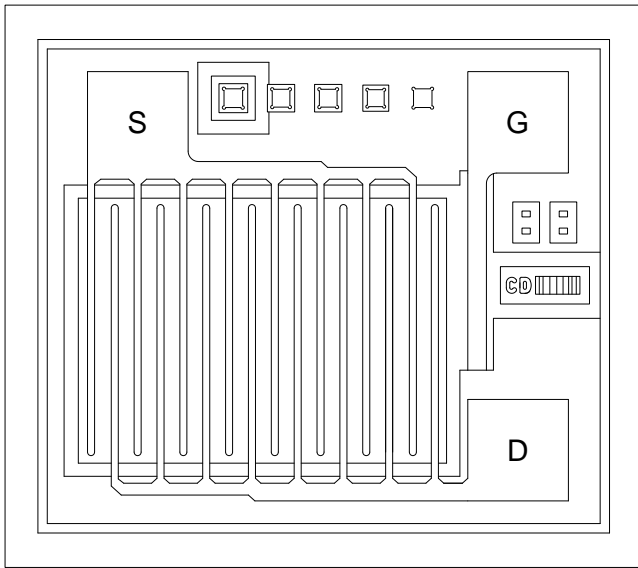
**Effective Date of Change:**

Existing Inventory of chip process CP688 will be shipped until depleted.

**Sample Availability:**

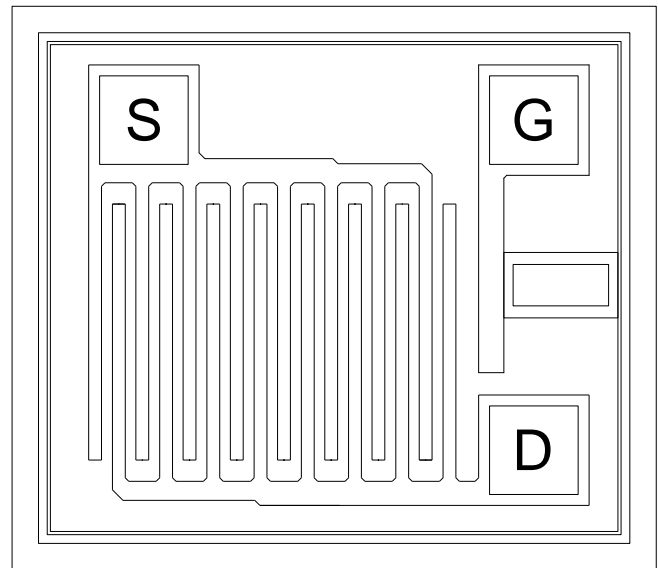
Please contact your salesperson or manufacturer's representative for samples.

**Figure 1: CP688 Chip Geometry (Discontinued)**



**BACKSIDE GATE**

**Figure 2: CP613V Chip Geometry**



**BACKSIDE GATE R0**

Wafer Diameter: 4 inch  
Die Size: 24 x 21 mils  
Die Thickness: 8.0 mils  
Bond Pad Size (Gate): 3.0 x 3.0 mils  
Bond Pad Size (Source): 3.0 x 3.0 mils  
Bond Pad Size (Drain): 3.0 x 3.0 mils  
Topside Metal: Al-Si (17,000Å)  
Backside Metal: Au-As (13,000Å)

Wafer Diameter: 5 inch  
Die Size: 24 x 21 mils  
Die Thickness: 7.1 mils  
Bond Pad Size (Gate): 3.3 x 3.3 mils  
Bond Pad Size (Source): 3.3 x 3.3 mils  
Bond Pad Size (Drain): 3.3 x 3.3 mils  
Topside Metal: Al-Si (17000Å)  
Backside Metal: Au-As (10000Å)

**Part Numbers Affected:**

CMPFJ175	CP688-CMPFJ176-WN
CMPFJ176	



145 Adams Avenue, Hauppauge, NY 11788 USA  
Tel: (631) 435-1110 • Fax: (631) 435-1824  
[www.centalsemi.com](http://www.centalsemi.com)  
<mailto:processchange@centalsemi.com>  
<http://www.centalsemi.com/processchange>

**PCN #172**  
**Notification Date:**  
**21 May 2019**

As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor's Product/Process Change Notification (PCN).

Company Name:	
Address:	
Printed Name:	
Title:	
Signature:	
Date:	