**Product / Process Change Notice**

**Parts Affected:**

Chip process, CP773, P-Channel Mosfets, wafers and bare die

**Extent of Change:**

The CP773 wafer process has been discontinued and replaced with the CP798X wafer process. See figures 1 and 2 for details.

**Reason for Change:**

The CP773 wafer has been replaced to the CP798X wafer process in order to enhance the manufacturing process controls and performance. In addition, this change is being done to ensure undisrupted supply of product, moving forward.

**Effect of Change:**

The wafer process meets all electrical specifications of the individual devices listed on the following page.

**Qualification:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | P/N: | CP798X Chip Process |  | Package: | SOIC-8 |
|  |  |  |  |  |  |  |
| **No.** | **Test** | **Conditions**(Reference standards are in bold) | **Qty** | **Pass/Fail** | **Test Results** |
| **1** | **Device Life Tests** |
|  | a | **High Temperature Gate Bias (HTGB)** | T=150°C, t = 1000 hours100% V\_GS**JESD22-A108** | 80 | Pass | 80/80 |
|  | b | **High Temperature Reverse Bias (HTRB)** | T=150°C, t = 1000 hours80% V\_DS**JESD22-A108** | 80 | Pass | 80/80 |

**Effective Date of Change:**

Existing inventory of Chip Process CP773 will be shipped until depleted.

**Sample Availability:**

Please contact your salesperson or manufacturer’s representative for samples.

**Figure 1: CP773 Chip Geometry (Discontinued) Figure 2: CP798X Chip Geometry**

 

Wafer Diameter: 8 inch

Die Size: 39 x 27 mils

Die Thickness: 7.5 mils

Bond Pad Size (Gate): 6.5 x 6.5 mils

Bond Pad Size (Source): 33 x 21 mils

Topside Metal: Al (40,000Å)

Backside Metal: Ti/Ni/Ag (1000Å/3000Å/10000Å)

Wafer Diameter: 8 inch

Die Size: 37.8 x 26 mils

Die Thickness: 5.5 mils

Bond Pad Size (Gate): 7.3 x 7.3 mils

Bond Pad Size (Source): 34 x 22.2 mils

Topside Metal: Al-Cu (40,000Å)

Backside Metal: Ti/Ni/Ag (1000Å/3000Å/10000Å)

**Part Numbers Affected:**

|  |  |
| --- | --- |
| CEN1232 | CP773-CMPDM302PH-WN |

As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor’s Product/Process Change Notification (PCN).

|  |  |
| --- | --- |
| Company Name: |  |
| Address: |  |
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|  |
| Printed Name: |  |
| Title: |  |
| Signature: |  |
| Date: |  |