**Product / Process Change Notice**

**Extent of Change:**

Chip process CP305, NPN silicon transistor wafers and bare die.

**Extent of Change:**

The CP305 wafer process has been discontinued and replaced with the CP306V wafer process. See figures 1 and 2 for details.

**Reason for Change:**

New wafer process provides an improved and consistent yield.

**Effect of Change:**

The wafer process meets all electrical specifications of the individual devices listed on the following page.

**Effective Date of Change:**

December 1, 2017

**Sample Availability:**

Please contact Salesperson or Manufacturer’s Representative.

**Qualification Tests:**

|  |  |  |
| --- | --- | --- |
| **Test** | **Condition** | **Failure rate** |
| **Resistance to Solder Shock**  | T =260⁰C ±5⁰CDwell time = 10 sec.**JESD22-B106** | 0/77 |
| **High Temperature Storage Life/ bake test.** |  150°C (-0/+10)°C, 1000 hours.**JESD22-A103** | 0/77 |
| **Temperature Cycling** | T= -65⁰C to +150⁰C1000 cycles. Dwell time = 15 min.**JESD22-A104** | 0/77 |
| **High Temperature Reverse Bias (HTRB)** | T=125⁰C, t=48 hours, 80% MAX rated VCB**JESD22-A108** | 0/77 |
| **Highly Accelerated Temperature and Humidity Stress Test (HAST)** | T = 130°C, RH = 85%, P = 33.3 psia, and t = 96 hours.Bias conditions per device specification sheet.**JESD22-A110** | 0/77 |
| **Accelerated Moisture Resistance Unbiased Autoclave** | Temperature = 121⁰C ± 2⁰C; relative humidity = 100%; vapor pressure = 205kPa, 29.7 psia. t=48 hours**JESD22-A102** | 0/77 |

**Figures:**

**Figure 1: CP305 Chip Geometry (Discontinued) Figure 2: CP306V Chip Geometry**

Wafer Diameter: 5 inch

Die Size: 27.56 x 27.56 mils

Die Thickness: 7.1 mils

Bond Pad Size (Emitter): 5.9 x 7.9 mils

Bond Pad Size (Base): 5.9 x 7.9 mils

Topside Metal: Al-Si (30,000Å)

Backside Metal: Au (9,000Å)

Wafer Diameter: 4 inch

Die Size: 31 x 31 mils

Die Thickness: 9.0 mils

Bond Pad Size (Emitter): 6.5 x 13.8 mils

Bond Pad Size (Base): 5.9 x 11.8 mils

Topside Metal: Al (30,000Å)

Backside Metal: Au (18,000Å)

**Part Numbers Affected:**

CP305-2N3019-CT

CP305-2N3019-CT20

CP305-2N3019-WR

CP305-2N3700-CT

As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor’s Product/Process Change Notification (PCN).

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| Company Name: |  |
| Address: |  |
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| Printed Name: |  |
| Title: |  |
| Signature: |  |
| Date: |  |