

Tel: 1.631.435.1110 Fax: 1.631.435.1824 **www.centralsemi.com**

mailto:processchange@centralsemi.com https://www.centralsemi.com/process-change-notices

PCN # 183 Notification Date: 18 May 2020

Product / Process Change Notice

Parts Affected:

Chip process CP390, N-channel MOSFETs, wafers and bare die

Extent of Change:

The CP390 wafer process is being replaced by the CP401 wafer process. See Figures 1 and 2 for details.

Reason for Change:

The CP390 wafer process is being replaced by the CP401 wafer process to enhance the manufacturing process controls and performance. This change will help ensure an undisrupted supply of product. The wafer size has increased from 6 inch to 8 inches in order to improve throughput.

Effect of Change:

The CP401 wafer process meets all electrical specifications of the individual devices listed on the following page.

Qualification:

P/N: CP401 Chip Process Package: DPAK

N	lo.	Test	Conditions (Reference standards are in bold)	Qty	Pass/Fail	Test Results
1		Device Life Tests				
	а	High Temperature Gate Reverse Bias (HTGB)	T=150°C, t = 1000 hours 100% VGS=30V JESD22-A110	45	Pass	45/45
	b	High Temperature Reverse Bias (HTRB)	T=150°C, t = 1000 hours VDS=600V JESD22-A108	45	Pass	45/45
	С	High Accelerated Temperature and Humidity Stress Test (HAST)	T=130°C, t = 96 hours, 85%RH, 230kPA, VDS=42V JESD22-A108	45	Pass	45/45
	D	Temperature Cycling (TC)	-65°C -+150°C, Tdwell ≥10min, 500 cycles	45	Pass	45/45

Page 1 of 3



145 Adams Avenue, Hauppauge, NY 11788, USA
Tel: 1.631.435.1110 Fax: 1.631.435.1824

WWW.Centralsemi.com

 $\underline{mailto:process change@centralsemi.com}$

https://www.centralsemi.com/process-change-notices

PCN # 183 Notification Date: 18 May 2020

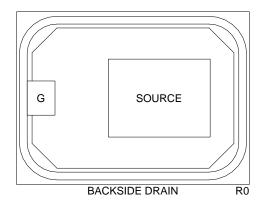
Effective Date of Change:

Existing inventory of chip process CP390 will be shipped until depleted.

Sample Availability:

Please contact your salesperson or manufacturer's representative for samples.

Figure 1: CP390 Chip Geometry



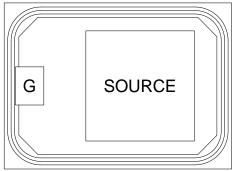
Wafer Diameter: 6 inch

Die Size: 117.0 x 87.4 mils

Die Thickness: 9.1 mils

Bond Pad Size (Gate): 14.0 x 17.3 mils Bond Pad Size (Source): 51.2 x 39.4 mils Topside Metal: Al (43,000Å) Backside Metal: Ag (8,000Å)

Figure 2: CP401 Chip Geometry



BACKSIDE DRAIN

Wafer Diameter: 8 inch

Die Size: 107.1 x 77.2 mils

Die Thickness: 9.1 mils

Bond Pad Size (Gate): 13.4 x 17.7 mils Bond Pad Size (Source): 51.2 x 51.2 mils Topside Metal: Al-Si (43,000Å) Backside Metal: Ag (8,000Å)

Part Numbers Affected:

CDM4-600LR	CP390-CDM4-600LR-CT
	CP390-CDM4-600LR-WN

Page 2 of 3



<u>mailto:processchange@centralsemi.com</u>
https://www.centralsemi.com/process-change-notices

PCN # 183 Notification Date: 18 May 2020

As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor's Product/Process Change Notification (PCN).

Company Name:	
Address:	
Printed Name:	
Title:	
Signature:	
Date:	

Page 3 of 3