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**PCN # 259**  
**Final Notification Date:**  
**November 14, 2024**

## Product / Process Change Notice

**Devices affected:**

All Devices manufactured in the DPAK Case.

**Extent of change:**

The lead frame has been re-tooled which resulted in a slight change in some of the mechanical dimensions (see figure 1).

**Reason for change:**

This change was instituted in order to continuing supporting future production of the DPAK case.

**Effect of change:**

This change does not affect the form, fit, or function of any device.

**Qualification data:**

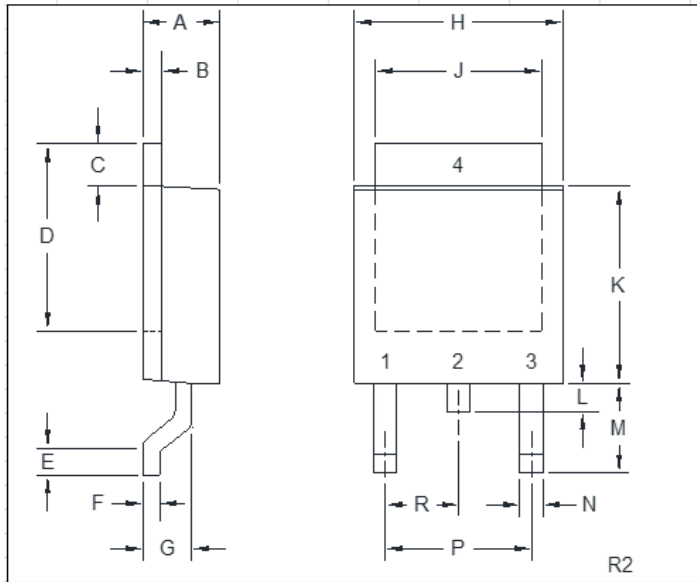
	Test Item	Test Condition	Sample Size	Failure Unit	Reference Standard
0	Pre-conditioning (For TC, AC, H3TRB, IOL, RSH)	1. TCT -55°C~+150°C 5Cycle 2. Bake 125 +5/-0 °C 24hrs 3. Humidity 85°C / 85%RH 168hrs 4. Reflow 3 Times 30s	338	0	JESD22-A113
1	High Temperature Reverse Bias (HTRB)	Ta = 100°C , V= 80% V <sub>R</sub> 1000hrs	77	0	JESD22-A108
2	Temperature Cycling (TC)	Ta = -55°C~+150°C, 2 cycles/hr, 1,000cycles	77	0	JESD22-A104
3	High Temperature Storage Test (HTSL)	Ta = 150°C 1000hrs	77	0	MIL-STD-750-1 METHOD-1032.2
4	High Humidity High Temp. Reverse Bias(H3TRB)	Ta=85°C/ 85%RH , V =80% V <sub>R</sub> (Max=100V) 1,000hrs	77	0	JESD22-A101
5	Autoclave (AC)	Ta = 121°C, P = 29.7psia ,100%RH 96hrs	77	0	JESD22-A102
6	Intermittent Operating Life (IOL)	T <sub>j</sub> ≥100°C Power On: 120 Sec ; Power Off: 120 Sec 15,000cycles	77	0	MIL-STD-750 Method 1037
7	Forward Surge Current (FSC)	SQ wave or sine wave;IFSM=datasheet Spec. Duration of pulses(tp)=8.3ms;1cycle	22	0	MIL-STD-750-4 METHOD 4066.6
8	Solderability (SD)	Temperature of solder pot = 245 ±5°C Time for dipping in solder = 5 ±0.5 Sec	10	0	J-STD-002
9	Resistance to Solder Heat (RSH)	Temperature of solder pot = 260+5/-0°C Time for dipping in solder = 10+2/-0Sec	30	0	JESD22-A111

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**Earliest effective date of change:**

February 14, 2025

**Figure 1 – DPAK Mechacical Dimensions**



DIMENSIONS								
SYMBOL	BEFORE CHANGE				AFTER CHANGE			
	INCHES		MILLIMETERS		INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.083	0.108	2.10	2.75	0.083	0.108	2.10	2.75
B	0.016	0.032	0.40	0.81	0.016	0.035	0.40	0.89
C	0.035	0.063	0.89	1.60	0.035	0.063	0.89	1.60
D	0.203	0.228	5.15	5.79	0.203	0.228	5.15	5.79
E	0.020	-	0.51	-	0.020	-	0.51	-
F	0.016	0.024	0.40	0.60	0.016	0.024	0.40	0.60
G	0.051	0.071	1.30	1.80	0.061		1.55	
H	0.248	0.268	6.30	6.81	0.248	0.268	6.30	6.81
J	0.197	0.217	4.95	5.50	0.195	0.217	4.95	5.50
K	0.209	0.245	5.30	6.22	0.209	0.245	5.30	6.22
L	0.025	0.040	0.64	1.02	0.033		0.83	
M	0.090	0.115	2.30	2.91	0.090	0.115	2.30	2.91
N	0.012	0.045	0.30	1.14	0.012	0.045	0.30	1.14
P	0.180		4.60		0.180		4.60	
R	0.090		2.30		0.090		2.30	



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As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor's Product/Process Change Notification (PCN).

Company Name:	
Address:	
Printed Name:	
Title:	
Signature:	
Date:	