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PCN #191
Notification Date:
June 19, 2020

Product / Process Change Notice

Parts Affected:

Chip process CP771, P-channel MOSFETs, wafers and bare die.

Extent of Change:

The CP771 wafer process has been discontinued and is being replaced with the CP805 wafer process. See Figures 1 and 2 for details.

Reason for Change:

The CP771 wafer process has been replaced in order to enhance manufacturing process controls and device performance. This change will help ensure an undisrupted supply of product.

Effect of Change:

The CP805 wafer process meets all electrical specifications of the individual devices listed on the following page.

Qualification:

P/N: CP805 Chip Process

Package: TO-220

No.	Test	Conditions (Reference standards are in bold)	Qty	Pass/Fail	Test Results
1	Device Life Tests				
A	High Temperature Gate Bias (HTGB)	T=150°C, t = 1000 hours 100% V _{GS} Negative Bias JESD22-A108	77	Pass	77/77
B	High Temperature Gate Bias (HTGB)	T=150°C, t = 1000 hours 100% V _{GS} Positive Bias JESD22-A108	77	Pass	77/77
C	High Temperature Reverse Bias (HTRB)	T=150°C, t = 1000 hours 100% V _{DS} JESD22-A108	77	Pass	77/77

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Effective Date of Change:

Existing inventory of chip process CP771 will be shipped until depleted.

Sample Availability:

Please contact your salesperson or manufacturer's representative for samples.

Figure 1: CP771 Chip Geometry (Discontinued)

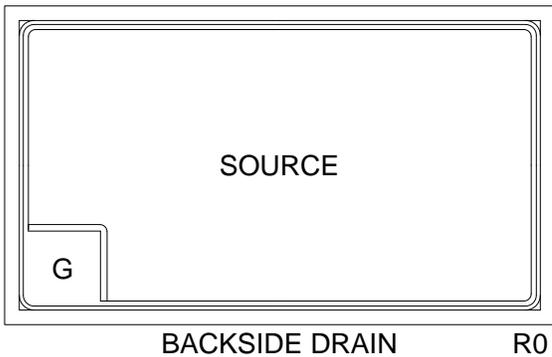
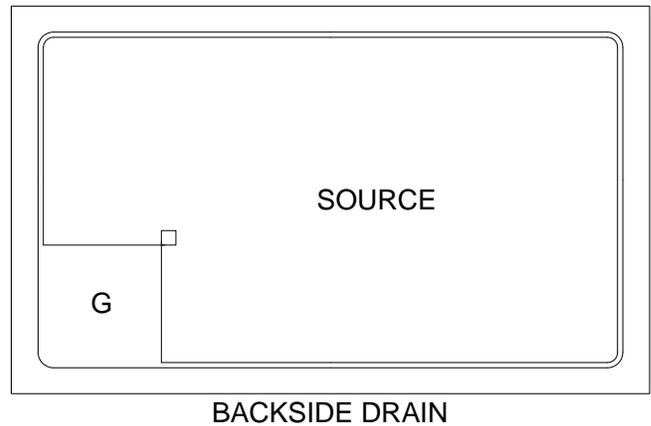


Figure 2: CP805 Chip Geometry



Wafer Diameter: 8 inch
Die Size: 55 x 32 mils
Die Thickness: 7.5 mils
Bond Pad Size (Gate): 7.3 x 7.3 mils
Bond Pad Size (Source): 50 x 25 mils
Topside Metal: Al (40,000Å)
Backside Metal: Ti/Ni/Ag (1,000Å/3,000Å/10,000Å)

Wafer Diameter: 8 inch
Die Size: 63.8 X 38.9 mils
Die Thickness: 5.5 mils
Bond Pad Size (Gate): 7.1 x 7.1 mils
Bond Pad Size (Source): 60.4 x 35.6 mils
Topside Metal: Al-Cu (40,000Å)
Backside Metal: Ti/Ni/Ag (1,000Å/3,000Å/10,000Å)

Part Numbers Affected:

CXDM4060P	CP771-CXDM4060P-CT
	CP771-CXDM4060P-WN



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As per JEDEC standard JESD46, Customer Notification of Product/Process Changes by Solid-State Suppliers, a lack of acknowledgement of a PCN within thirty (30) days constitutes acceptance of the change.

The undersigned acknowledges and accepts Central Semiconductor's Product/Process Change Notification (PCN).

Company Name:	
Address:	
Printed Name:	
Title:	
Signature:	
Date:	