What is a Current Limiting Diode?

A Current Limiting Diode, also known as a “Current Regulating Diode” or a “Constant Current Diode”, performs quite a unique function. Similar to a zener diode, which regulates voltage at a particular current, the CLD limits or regulates current over a wide voltage range. The CLD is diffused using a “Field Effect” process similar to the diffusion techniques used in manufacturing JFETs with the electrical characteristics optimized for high output impedance and current regulating capability.

How Does a Current Limiting Diode Operate?

In operation the CLD regulates the amount of current that can flow over a voltage range of about 1 to 100 volts. The equivalent circuit of the CLD is a current generator in series with a parallel combination of the dynamic impedance and the junction capacitance (Figure 1).

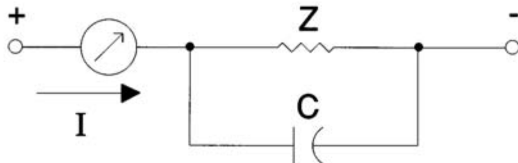

Figure 1. The CLD Equivalent Circuit

The shunt capacitance of Central's CLD is about 4-10 pF over the useful operating voltage range.

Outline below are typical CLD Characteristics, Symbols, Parameters and Definitions.

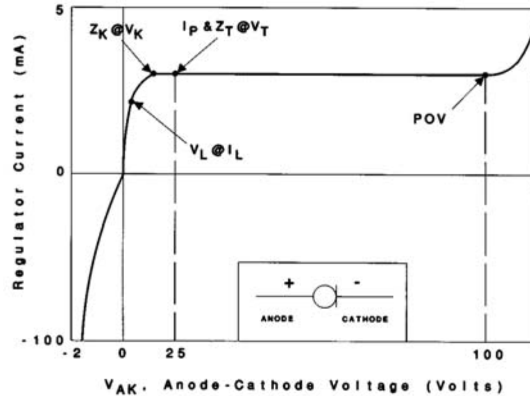

Figure 2. CLD Characteristic Curve

I_L - Limiting Current: 80% of I_P minimum used to determine Limiting Voltage V_L.

I_P - Pinch-off Current: Regulator current at specified Test Voltage (V_T = 25V).

POV - Peak Operating Voltage: Maximum voltage to be applied to device.

TC - Current Temperature Coefficient.

V_{AK} - Anode to Cathode Voltage.

V_K - Knee Impedance Test Voltage: Specified voltage used to establish Knee Impedance (Z_K).

V_L - Limiting Voltage: Measured at I_L, V_L together with knee AC impedance (Z_K), indicates the knee characteristics of the devices.

V_T - Test Voltage: Voltage at which I_P and Z_T are specified.

Z_K - Knee AC impedance at Testing Voltage:To test for Z_K, a 90 Hz signal (V_K), with RMS value equal to 10% of the test voltage, V_K, is superimposed on V_K: $Z_K = V_K/i_K$, where i_K is the resultant AC current due to V_K To provide the most constant current, Z_K should be as high as possible.

Z_T - AC Impedance at Test Voltage: Specified as a minimum value. To test for Z_T, a 90 Hz signal with RMS value equal to 10% of Test Voltage (V_T), is superimposed on V_T.

As shown by the characteristic curve (Figure 2) and cross sectional diagram (Figure 3), the CLD begins to conduct when a reverse biased voltage is applied from the cathode to the anode or PN junction. As the reverse biased voltage is increased to V_L, the current increases due to the bulk resistance of the N region. As the current approaches the knee section of the curve, a depletion region develops between the N region and the P-type gate. This depletion region decreases the current path in the N region slowing the increase of current flow. Eventually, the depletion region meets the P-type gate and pinch-off occurs, allowing current flow to become constant and almost independent of applied voltage until PN junction breakdown occurs somewhere above POV. When the polarity of the applied voltage is reversed and a forward bias is applied to the PN junction, the CLD exhibits characteristics similar to those of a forward biased diode or rectifier.

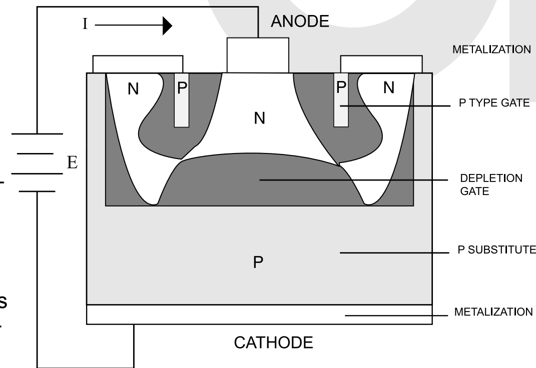

Figure 3. CLD Chip Cross Section

Thermal Considerations

Central Semiconductors CCL0035 thru CCL5750 series of current limiting diodes covers a current range of 35µA to 5.75mA in 12 different current groups. These devices operate over a temperature range of -65°C to +200°C and have a moderate temperature coefficient that can cause Ip drift. This Ip drift can sometimes be a problem if not taken into account when designing precision circuitry that must operate over a wide temperature range. The Ip drift phenomenon becomes more evident with higher current CCL types because the temperature coefficient increases and the heating due to power dissipation is greater.

Outlined at right: Calculations of Ip change for two CCL types assuming heating is due to device dissipation only.

Type	I_P(nom)	TC(max)	Dissipation @25V	ΘJL	ΔI_P	
					%	mA
CCL1000	1.1mA	-0.37%/°C	27.5mW	200°C/W	-2.03	-0.022
CCL5750	5.57mA	-0.53%/°C	143.75mW	200°C/W	-15.2	-0.876

In most applications the absolute value of the current need not be precise as long as it is constant and in the desired range. However, the Ip drift can cause correlation problems between vendor and customer if testing is not specified precisely.

Variations in Ip Measurement vs. Test Method

There are two basic methods of measuring Ip: Pulse and DC steady state. Pulsed testing is accomplished using computerized test equipment with a programmed test time in the millisecond area. DC steady state testing is accomplished using a 90-second dwell time with the device leads connected to an infinite heat sink 0.375 inches from the body. Central Semiconductor uses the pulsed test technique because of it's accuracy, repeatability and speed. The DC steady state method will not correlate well with the pulse method at the higher current levels due to effects of heating.