Practical Applications of Current Limiting Diodes

By Joe Chan, Central Semiconductor Corp.

The current limiting diode (CLD) or current regulating diode (CRD) has been available since the early 1960's. Unfortunately, despite its simplicity and distinct advantages over conventional transistorized applications, it has seen only limited use. One reason may be designers' lack of familiarity with practical circuit design techniques involved with its use. Another reason may be that although many papers have been published on the device, most have dealt primarily with solid-state theory rather than with practical applications. Therefore, it is the purpose of this paper to focus on how this device is used, rather than on what it is.

Conventional Constant Current Source vs. CLD

From basic circuit theory, an ideal current source is one with infinite output impedance. The term constant current source usually applies to a circuit that supplies a DC current whose amplitude is independent of a change in either load or supply voltage.

**Basic Constant Current Circuit**

The simplest circuit is a voltage source in series with a resistor as shown on Fig. 1. The current is \( I = \frac{V_s}{R} \). The current would change very little if the load voltage, \( V_L \), is small compared with the supply voltage, \( V_s \), and the source resistance, \( R_s \). When the load voltage is in the order of several volts and accuracy within a few percent is required, the circuit in Fig.1 can be achieved only if \( V_s \) has a magnitude of several hundred volts. This may be feasible, but is impractical.

**Transistor Constant Source**

For a constant current source, the use of a transistor as shown in Fig.2 would eliminate the need for a high voltage source. This circuit provides a constant current of approximately 10 mA, which is determined by the current through \( R_1 \), and in turn on the voltage across \( R_2 \). The load current, \( I_L \), is also \( V_s/(R_2 + R_3) \). This current will maintain its constant amplitude provided the transistor is not saturated, i.e. \( V_t < V_s/(R_2 + R_3) \).

As the load, \( R_L \), changes, the collector voltage of \( Q_2 \) will change, but the collector current will change very little because its dynamic impedance, \( r_c \), is very large, typically at 1 MΩ. The transistor operates like a constant current source with resistance, \( r_c \). A non-transistor source would require a supply in the range of hundreds of volts to equal this performance.

Even though the Fig. 2 circuit represents a great improvement over that of Fig. 1, there are still limitations on its performance, such as temperature drift associated with both resistor and transistor parameters, notably the \( V_t \) and the leakage \( I_C \). Also, any variation of \( V_s \) will cause a change in the bias voltage; therefore, will affect the constant current.

**Stabilized Current Source**

Fig. 3 shows a stabilized version of the Fig. 2 circuit. In this circuit, a zener diode replaces \( R_3 \) of Fig. 2. The zener is equivalent to a battery in series with a low resistance, \( R_z \), which is typically 20Ω. This current has great stability against variation in the supply voltage, \( V_s \). In the Fig. 2 circuit, 50 percent \( [R_2/(R_2 + R_3)] \) of the change in \( V_s \) would affect the \( Q_2 \) bias, whereas in the Fig. 3 circuit, only 0.04 percent \( [R_2/(R_2 + R_3)] \) of a \( V_s \) change is felt on the \( Q_2 \) bias.

A low temperature coefficient zener may be used in this circuit. Many zeners with temperature coefficients of ±0.1%/°C or less are available. To further improve stability against temperature drift, a diode may be added in series with the zener, thus compensating for the \( V_t \) drift.

**Fig. 1. Basic Constant Current Circuit**

**Fig. 2. Transistor Constant Current Circuit**

**Fig. 3. Stabilized Constant Current Source Circuit**

**Fig. 4a. FET Current Source Characteristics**

**Fig. 4b. CLD Volt-Ampere**
**Current Limiting Diode (CLD)**

The CLD or constant current diode is basically a junction FET transistor operating with its gate shorted to the source terminal, as shown in Fig. 4a. In this configuration, the JFET exhibits a unique current-limiting characteristic as $V_{DS}$ is increased until the FET's voltage breakdown limit is reached. This current-limiting characteristic is shown in Fig. 4b. In order to explain the Fig. 4b characteristics, a cross-section of the N-channel JFET is shown in Fig. 5a.

When the drain current begins to flow as $V_{DS}$ is applied, a voltage drop, $V_{RDS}$, is developed along the channel. This voltage drop provides a reverse bias on the PN junction. Hence, the depletion regions grow until they meet, at which point any further increase in $V_{DS}$ will be counter-balanced by an increase in the depletion region voltage drop. When this condition is reached, the current has reached its limiting condition. The $V_{DS}$ voltage that causes the current to reach limiting condition is called $V_{PL}$, the pinch-off voltage.

In this configuration, transistors $Q_1$ and $Q_2$ are assumed identical, $R_S = R_{S1} = R_{S2}$, and $R_E > R_z$. Hence, $V_{PL}$ is changed from $1/2 e_{in1}/(R_L + R_S + R_E)$ to $1/2 e_{in1}/(R_L + (R_S + R_E))$ and $V_{PL}$ thus is slightly smaller. $Q_1$'s emitter current therefore is increased, and $Q_2$'s emitter current is decreased. This implies that $Q_2$'s gain is higher. With regard to the source signal $e_{in}$, its effect is equal but opposite to that of $e_{in1}$. Hence

$$v_{RL} / e_{in1} = 1/2 R_s = (1/2 R_L + (R_S + R_E))/R_L$$

The voltage gain of $Q_2$ is the same as $Q_1$, but opposite in sign.

If the bias resistor, $R_z$, is finite, it has a parallel effect on the impedance $R_L + R_S + R_E$, hence $V_{PL}$ is changed from $1/2 e_{in1}/(R_L + (R_S + R_E))$ to $1/2 e_{in1}/(R_L + R_z + (R_S + R_E))$, and $V_{PL}$ thus is slightly smaller, $Q_1$'s emitter current therefore is increased, and $Q_2$'s emitter current is decreased. This implies that $Q_2$'s gain is higher. With regard to the source signal $e_{in}$, its effect is equal but opposite to that of $e_{in1}$.

**Differential Amplifiers**

Today's most popular amplifier is the differential amplifier because, theoretically, it responds only to the difference of two signals, and is inherently temperature stable. The common-mode rejection ratio, CMR, is normally a measure of its performance — i.e., the higher the CMR, the better a device's performance. Presented in Fig. 6 is a standard differential amplifier circuit and in Fig. 7 is an AC equivalent circuit, which will be used to show how the CMR may be greatly improved by incorporating a CLD to provide a common bias current.

For $Q_2$, since the emitter current is the same:

$$v_{RL} / e_{in1} = 1/2 R_L/(R_z + (R_S + R_E))/R_L$$

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If the bias resistor, $R_z$, is finite, it has a parallel effect on the impedance $R_z + R_L + R_S$, hence $V_{PL}$ is changed from $1/2 e_{in1}/(R_L + R_z + R_S)$ to $1/2 e_{in1}/(R_L + (R_z + R_S))$, and $V_{PL}$ thus is slightly smaller, $Q_1$'s emitter current therefore is increased, and $Q_2$'s emitter current is decreased. This implies that $Q_2$'s gain is higher.

With regard to the source signal $e_{in}$, its effect is equal but opposite to that of $e_{in1}$. Hence

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With both $e_{in1}$ and $e_{in2}$ present, the output voltage can be shown by superposition to be:

$$V_{out} = -1/2 e_{in1} \left( \frac{R_L}{R_L + R_S + R_E} \right) + 1/2 e_{in2} \left( \frac{R_L}{R_L + (R_S + R_E)} \right)$$

It follows that:

$$v_{RL} = -1/2 \left( e_{in1} - e_{in2} \right) \frac{R_L}{R_L + (R_S + R_E)} , \quad \text{and} \quad v_{RL} = -1/2 \left( e_{in1} - e_{in2} \right) \frac{R_L}{R_L + (R_S + R_E)}$$

The above shows that if $e_{in1} = e_{in2}$, then $v_{RL} = 0$, and if $e_{in1} = -e_{in2}$, then the above becomes

$$v_{RL} = e_{in1} \left( \frac{R_L}{R_L + (R_S + R_E)} \right) , \quad v_{RL} = e_{in2} \left( \frac{R_L}{R_L + (R_S + R_E)} \right)$$

The amplifier thus produces equal and opposite outputs based upon the difference between the two input signals, but independent of their sum.

When a differential amplifier is used to measure the difference of two signals, the criteria for performance is the ratio of the gain due to the difference to the gain due to the sum of the two input signals, known as common mode rejection, or CMR.

$$\text{CMR} = \frac{V_{out}(e_{in1} - e_{in2})}{V_{out}(e_{in1} + e_{in2})} = \frac{2 R_z}{(R_L + R_S + R_E)}$$

For the Fig. 6 circuit, $1/2 R_z = 50k\Omega$, so

$$\text{CMR} = \frac{2 \times 50k\Omega}{(R_L + R_S + R_E)}$$

If $e_{in1} = e_{in2}$, the signal is zero, and the CMR is infinity. The CMR of an op-amp is defined as

$$\text{CMR} = \frac{V_{out}(e_{in1} - e_{in2})}{V_{out}(e_{in1} + e_{in2})} = \frac{2 \times 50k\Omega}{(R_L + R_S + R_E)}$$

If a 1 mA CLD is used for $R_z$, as shown in Fig. 8 (page 52), and since the Zd for such a CLD is typically 1 Meg $\Omega$.

One can see the significant improvement in CMR by a factor of more than 100X with the CLD.

**Market Availability of CLD’s**

Today, CLD's are available with current ranges from 35 $\mu$A to 15 mA, and associated impedance values from over 20 M$\Omega$ to several hundred K$\Omega$. The use of CLD's is limited only by one's imagination in the application of the basic laws of electronics.

**Current Amplification & Division**

Even though the current range of the CLD is limited to less than 15mA, this current may be practically amplified to a higher level. Shown in Fig. 9 is a circuit using an op-amp to either amplify or attenuate a CLD's current level.

Since an ideal op-amp has infinite input impedance, its input currents $I_{IN} + I_{IN}$ are zero, and its differential input $V_{IN} = 0$. Therefore,

$$V_{IN} = V_{OUT}$$

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Hence $I_{CLD} = V_{IN} = \frac{V_{OUT}}{R_z}$

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This shows that the CLD's current level may be amplified or attenuated by the ratio of resistors $R_1$ and $R_2$. The maximum load current is limited by the Op Amp's current capacity, i.e., for a given $I_{CLD}$, the maximum $R_2$ is limited by the input voltage rating of the Op Amp, such that $I_{OUT} < max$ input voltage rating.

There are many Op Amps available with current ratings up to several hundred mA, and with input voltage ratings up to 15 V. Their input voltage offsets range from a few nV down to a few pV, and input offset currents from 1 μA down to less than 1 nA. Hence the use of a high performance Op Amp provides very accurate current amplification or attenuation. Assume, for example, that $I_{CLD} = 1 mA$, $R_1 = 1 K$ and $R_2 = 100$. If $R_1/R_2 = 10$, the use of a high performance Op Amp provides very accurate current amplification or attenuation.

### Resistance Measurement

The Current Amplifying/Dividing Technique shown above may be easily applied to resistance measurement. The measurement circuit, if digitally controlled and programmed, may become part of an automatic test equipment (ATE) system.

From the basic formula $V_x = I_{CLD} R_x$, the voltage $V_x$, is proportional to the unknown resistance $R_x$. If $I_{CLD}$ is known, the unknown $R_x$ may be found by reading the voltage $V_x$. Referring to the Fig. 9 circuit, if we select $R_1$ such that $I_{CLD} R_1 = V_x$, the voltage on $R_2$ is also $V_x$.

Hence $I_{S} R_2 = V_x$

If $R_2$ is selected in multiples of 10, and $V_x$ is limited to 1 V maximum, then the unknown, $R_x$, may be read directly on a decimal scale.

For example if $R_2$ is:

- $100 \Omega$, $R_x = 100 V_x$
- $1,000 \Omega$, $R_x = 1,000 V_x$
- $10,000 \Omega$, $R_x = 10,000 V_x$
- $100,000 \Omega$, $R_x = 100,000 V_x$
- $1,000,000 \Omega$, $R_x = 1,000,000 V_x$

The above shows that if the five resistor values from $100 \Omega$ to $1 M\Omega$ are incorporated for $R_2$, effectively the circuit of Fig. 9 is now transformed into a resistance-measuring circuit with 5 decimal scales capable of measuring resistances up to $1 M\Omega$ in five ranges. Fig. 10 shows such a transformed circuit with discrete components and values.

This circuit may be automated with an A-D converter to convert $V_x$ into Digital Data. Selection of the proper scale may be achieved through auto-ranging techniques under digital control.

### Voltage Amplitude Reference

When a known constant current flows through a known resistor, a known voltage is generated. This may be used as a reference (as shown in Fig. 11a) in many feedback control applications such as DC regulation, motor speed control, automatic frequency control, and automatic gain control. When the voltage reference is switched on and off, as shown on Fig. 11b, it becomes a pulse with a known reference amplitude, which can be used in a pulse-generator design.

#### Ultra High-Speed Pulse Amplitude

Shown in Fig. 12 is a high-speed pulse amplitude reference circuit. The amplitude of 1 V is generated by a 30 mA CLD through 100 ohms. The rise and fall times are less than 10 nS, achieved with the use of Schottky diodes as switches, driven by an ultra-high-speed op-amp.

In this circuit, the Op Amp, $U_1$, is driven by a digital TTL pulse signal. When the signal goes to logic “0”, $U_1$’s output goes high, and diode $D_2$ is reverse-biased and turned off, thus allowing the constant current through diode $D_2$, onto $R_2$. As the TTL signal goes high, $U_1$’s output goes low, thus forward-biasing $D_2$ and reverse-biasing $D_3$. Hence, the current to $R_2$ is switched off. The result is a reference pulse with precision amplitude.

### Other Applications

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would save the manufacturer time and money. As shown in Fig. 13b, the $V_C$ amplitude is proportional to time. At time $T_1$, the $V_C$ level is at $V_1$. If $T_1$ represents the transistor’s maximum $T_{on}/T_{off}$ time, then we can use $V_1$ as a reference for comparison with the peak voltage of a ramp corresponding to $T_{on}/T_{off}$ time of the transistor under test. If the $V_{pk} > V_1$, the detection circuit’s output would indicate failure, or vice versa. Fig. 15 shows a simplified version of such a detection circuit.

**Pulse Width Modulation**

When a sawtooth or triangular signal is compared with a DC signal, a pulse signal may be generated. The pulse width, $PW$, may be varied or modulated if the level of the DC signal is varied.

Shown in Fig. 16a is a simple pulse width modulator (PWM), with output waveforms for two DC signal levels shown in Fig. 16b. This pulse width modulator may be used as part of any feedback loop to control the proper function of an electronic apparatus such as a servo amplifier, switching regulator, phase controller, or a voltage-controlled oscillator.

Using a switching regulator as an example, its DC output is proportional to the duty cycle of the switching device that chops its DC input signal. When its DC output is compared with a reference sawtooth through a pulse width modulator, the pulse width of the PWM will vary in such a way that the DC output is maintained within its accuracy range. Shown in Fig. 17 is a simplified sketch of a PWM used within a switching regulator.

**Staircase Generator**

A staircase waveform may be generated through the use of a sample and hold technique as shown in Fig. 18a. If various levels along the ramp are sampled and held, a staircase waveform is generated as shown in Fig. 18b. The length of each step depends on the droop rate of the sample and hold amplifier. Using a Burr Brown SHC5320 device as an example, with a droop rate of ±0.5mv/mSec max, output voltage range of ±10V, and acquisition time of 1.5 µS max, a staircase waveform is generated that can be used for voltage level control or discrimination.

**Conclusion**

The Current Limiting Diode, offering simplicity and high performance characteristics when compared with a bipolar transistor, has been shown to offer versatility in many circuit applications, as well as superior performance regarding temperature drift and dynamic impedance.

**References:**

1. Field-Effect Transistors
   Walmark and Johnson, Prentice-Hall, 1966
2. Field-Effect Transistors
3. Operational Amplifiers
   Tobey, Graen, Hudsman, McGraw Hill, 1971
4. Electronic Designer’s Handbook
   T.K. Hemingway, Tab Books, 1967
5. Motorola Semiconductor Data Book, 1969

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